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EXAMINER	
HOLLINGTON, JERMELE M	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 08/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,449	CONTI ET AL.	
	Examiner	Art Unit	
	Jermele M. Hollington	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed June 27, 2006 have been fully considered but they are not persuasive.

The applicants argue: *"Iino et al do not monitor temperature or continuously vary voltage to maintain current at or below a set point. Such is taught and claimed in the present application. Iino et al do not have a bum in oven or a way to mount each chip individually (only the entire wafer as a whole). Moreover, in Iino et al, the power supply is turned off if an over voltage is detected. Since only one power supply 40 is shown (Col. 9, lines 25 and 26), apparently the power supply is shut off to every chip... Turning now to the claims, method claims 1 and 2 and structural counterpart claims 7 and 8 each require at least one chip to be burned in and mounted individually in a tool having a device for mounting each chip individually, and a source of electrical current individually to bum in each chip, and a monitor to monitor the temperature of each chip. These limitations are not shown or taught in Iino et al. Also, claims 1, 2, 7 and 8 require monitoring at least current, or voltage or power levels, and varying the voltage to each chip to maintain at least one of the values below a given level. As explained above, Iino et al do not monitor temperature, or vary the voltage in response thereto to maintain one of the values measured below a given value. Iino et al merely turn off the power supply when an over current is detected. This is quite different from applicants' teaching and claims."*

2. In response to the above arguments, the examiner disagrees that Iino et al do not disclose varying the voltage. Iino et al disclose in col. 4, lines 25-47, col. 5, lines 3-39 and col. 9, lines 25-26 that it is either reducing the voltage or shut off the voltage when the voltage exceeds the require voltage. Regarding monitoring the temperature, this claim is considered to be a Jepson claim (see MPEP 2129 for details) base on its structure. With a Jepson claim, the preamble is considered admitted prior art. Furthermore, the recitation "...a monitor...to continuously monitor the temperature valve of each chip..." has not been given patentable weight because the

recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

The applicants further argue: *"The Hamilton patent is controlling power to the heater that is attached to the heat sink; it is not controlling the voltage or current to the device or chip that is being burned in, as is taught and claimed herein. The heat sink and heater assembly are part of the burn in equipment, typically in practice attached to the bum in socket, bum in board or the oven. Applicants' invention involves varying the voltage or current applied to the chips. After burning in the chip, it is removed from the bum in equipment and shipped to the customer. Applicants acknowledged in the application that there are many known ways to control the temperature of a heat sink. The Hamilton patent is one way. Other prior art involves controlling air or fluid flow or temperature, or using thermoelectric devices. Thus, Hamilton has nothing to do with the present invention. Hence, further discussion of Hamilton is not believed to be warranted."*

In response to the above arguments, the examiner disagrees that Hamilton does not control the voltage or current of the device to be burn-in. The controller is controller circuit 64 that controls the voltage of the device burn-in 9see also col. 5, lines 26-44. Further, applicant's arguments do not comply with 37 CFR 1.111(c) because they do not clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. Further, they do not show how the amendments avoid such references or objections.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4 and 7-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Iino et al (5568054).

Regarding claims 1-2, Iino et al disclose [see Fig. 6] controlling the burning in of at least one I/C chip (IC chip on wafer W) in a burn in tool (inspection section 12), wherein said tool (12) has a device (probe card 20) for mounting each chip (IC on wafer W) to be burned in, and a power source (power source 40) to supply electrical current to burn in each chip (IC on wafer W), comprising the steps of: continuously monitoring [via measuring section 41] at least one electrical value input to each chip (on wafer W) wherein the current value is maintain at or below a given value [see col. 2, lines 9-30, col. 5, lines 3-63, col. 6, lines 29-37 and col. 7, line 47-col. 8, line 13].

Regarding claim 3, Iino et al disclose [see Fig. 6] at least one electrical value input to each chip (on wafer W) wherein the power value is maintain at or below a given value [see col. 2, lines 9-30, col. 5, lines 3-63, col. 6, lines 29-37 and col. 7, line 47-col. 8, line 13].

Regarding claim 4, Iino et al disclose each device temperature is monitored [via measuring section 41] and the voltage to each device (20) is varied to maintain the device temperature [see col. 2, lines 9-30, col. 5, lines 3-63, col. 6, lines 29-37 and col. 7, line 47-col. 8, line 13].

Regarding claims 7-8, Iino et al disclose [see Fig. 6] controlling the burning in of at least one I/C chip (IC chip on wafer W) in a burn in tool (inspection section 12), wherein said tool (12) has a device (probe card 20) for mounting each chip (IC on wafer W) to be burned in, and a power source (power source 40) to supply electrical current to burn in each chip (IC on wafer W), comprising the steps of: continuously monitoring [via measuring section 41] at least one electrical value input to each chip (on wafer W) wherein the current value is maintain at or below a given value [see col. 2, lines 9-30, col. 5, lines 3-63, col. 6, lines 29-37 and col. 7, line 47-col. 8, line 13].

Regarding claim 9, Iino et al disclose [see Fig. 6] at least one electrical value input to each chip (on wafer W) wherein the power value is maintain at or below a given value [see col. 2, lines 9-30, col. 5, lines 3-63, col. 6, lines 29-37 and col. 7, line 47-col. 8, line 13].

Regarding claim 10, Iino et al disclose a monitor (measuring section 41) to continuously monitor the temperature value of each chip (W) being burned in and wherein the voltage is varied to maintain the temperature value of each device at a given value [see col. 2, lines 9-30, col. 5, lines 3-63, col. 6, lines 29-37 and col. 7, line 47-col. 8, line 13].

3. Claims 1,4-7, and 10-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Hamilton (5911897).

Regarding claim 1, Hamilton discloses [see Figs. 1-2] a method of controlling the burning in of at least one I/C chip (IC chip 12) in a burn in tool (burn-in board 10), wherein said tool (10) has a device (heat sink assembly 24) for mounting each chip (12) to be burned in, and a power source (V REF in Fig. 3) to supply electrical current to burn in each chip (12), comprising the steps of: continuously monitoring [via sensor housing 44] at least one electrical value input to

each chip (12) selected from the group of current, voltage and power, and varying the voltage to maintain at least one of the values at or below a given value [see also col. 1, lines 45-56].

Regarding claim 4, Hamilton discloses each device temperature is monitored [via temperature sensor 48] and the voltage to each device is varied to maintain the device (24) at or below a given temperature.

Regarding claim 5, Hamilton discloses a heat sink (heat sink 34) in contact with the device (24).

Regarding claim 6, Hamilton discloses the device temperature of each device (24) is monitored [via temperature sensor 48] and the temperature of the heat sink (34) is varied to maintain the device temperature at a given value.

Regarding claim 7, Hamilton discloses a burn in tool (burn in board 10) for burning in at least one I/C chip (IC chip 12) comprising: a structure (heat sink assembly 24) for mounting each chip (12) to be burned in; a power source (V REF) to supply electrical current to burn in each chip (12); a structure (sensor housing 44) for continuously monitoring at least one electrical value input to each chip (12) selected from the group of current, voltage and power, and a structure to vary the voltage to maintain at least one of the values at or below a given value.

Regarding claim 10 Hamilton discloses a monitor (temperature sensor 48) to continuously monitor the temperature value of each chip (12) being burned in and wherein the voltage is varied to maintain the temperature value of each device at a given value.

Regarding claim 11, Hamilton discloses a heat sink (heat sink 34) is in contact with each device (24).

Regarding claim 12, Hamilton discloses the tool (10) has a heat sink (heat sink 34) and temperature monitor (48) for each device (24) and each heat sink (34) has means (48) to control the temperature of the heat sink (34), and the temperature control means (22) is varied to maintain the temperature value of each device (24) at a given value.

Conclusion

Base on the arguments, the following is being applied.

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jermele M. Hollington whose telephone number is (571) 272-1960. The examiner can normally be reached on M-F (9:00-4:00 EST) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha Nguyen can be reached on (571) 272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jermele M. Hollington
Primary Examiner
Art Unit 2829

JMH
August 30, 2006